10/727474



LSI LOGIC

# FAX COVER SHEET

LSI LOGIC CORPORATION
Office of General Counsel
1621 Barber Lane
M/S D-106
Milpitas, CA 95035
Fax: (408) 433-7460





**Date:** November 3, 2005

**To**
**Name:** USPTO – MS: Certificate of Correction
**Fax:** 571-273-8300
**Phone:** 703-305-8283

**From:**
**Name:** Manu Kashyap, Intellectual Property Paralegal
Corporate Legal Dept.
**Telephone:** (408) 433-7475
**Fax:** (408) 433-7460

Re: 6,954,082

Number of Pages Including this Page 4



***MESSSAGE:***

**Docket Number: 03-1681**
**Box: Certificate of Correction**

**Please notify us immediately if any pages are not received.**

RECEIVED
CENTRAL FAX CENTER

NOV 0 3 2005

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

# TRANSMITTAL FORM

*(to be used for all correspondence after initial filing)*

Total Number of Pages in This Submission: 3

| | |
|---|---|
| Application Number | 6,954,082 B2 |
| Filing Date | October 11, 2005 |
| First Named Inventor | Carlo Grilletto |
| Art Unit | 2829 |
| Examiner Name | Nguyen, Tu |
| Attorney Docket Number | 03-1681 |

## ENCLOSURES (Check all that apply)

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation
- ☐ Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please identify below):
  Certificate of Correction

Remarks

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

| | | | |
|---|---|---|---|
| Firm Name | LSI Logic Corporation | | |
| Signature | | | |
| Printed name | Timothy Croll | | |
| Date | November 3, 2005 | Reg. No. | 36,771 |

## CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

| | | | |
|---|---|---|---|
| Signature | | | |
| Typed or printed name | Manu Kashyap | Date | November 3, 2005 |

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

# UNITED STATES PATENT AND TRADEMARK OFFICE
## CERTIFICATE OF CORRECTION



PATENT NO. : 6,954,082 B2

APPLICATION NO.: 10/727,474

ISSUE DATE : October 11, 2005

INVENTOR(S) : Carlo Grilletto

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page at column 12, please delete "Grillettc" and replace with - Grilletto -

On the cover page at column 75, please delete "Grillettc" and replace with - Grilletto -

MAILING ADDRESS OF SENDER (Please do not use customer number below):

LSI Logic Corporation
1621 Barber Lane, MS: D-106
Milpitas, CA 95035 U.S.A.

Should be "Grilletto"

US006954082B2

(12) **United States Patent**
Grillette

(10) **Patent No.: US 6,954,082 B2**
(45) **Date of Patent: Oct. 11, 2005**

Should Be "Grilletto"

(54) **METHOD AND APPARATUS FOR TESTING OF INTEGRATED CIRCUIT PACKAGE**

(75) Inventor: Carlo Grillette, San Carlos, CA (US)

(73) Assignee: LSI Logic Corporation, Milpitas, CA (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/727,474

(22) Filed: Dec. 4, 2003

(65) Prior Publication Data

US 2005/0122127 A1 Jun. 9, 2005

(51) Int. Cl.[7] ..... G01R 31/26
(52) U.S. Cl. ..... 324/765
(58) Field of Search ..... 324/760, 754, 324/755, 757, 765, 158.1, 761, 763

(56) References Cited

U.S. PATENT DOCUMENTS

5,742,168 A * 4/1998 Kiyokawa et al. ..... 324/754
6,287,878 B1 * 9/2001 Maeng et al. ..... 438/15
6,597,189 B1 7/2003 Grilletto
6,750,646 B1 * 6/2004 Voss et al. ..... 324/158.1

OTHER PUBLICATIONS

IPC-9701, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," IPC—Association Connecting Electronics Industries, cover page.

* cited by examiner

*Primary Examiner*—Vinh Nguyen
*Assistant Examiner*—Tung X. Nguyen
(74) *Attorney, Agent, or Firm*—L. Jon Lindsay

(57) **ABSTRACT**

A method and apparatus for testing an integrated circuit (IC) package includes a printed circuit board (PCB) on which is mounted the IC package and which is removably connected (preferably perpendicular) to a motherboard. The IC package, the PCB and the motherboard are subjected to thermal, humidity and/or electrical test conditions.

**20 Claims, 4 Drawing Sheets**